ABSTRACT OF THE DISCLOSURE

A large number of pixels PXL are arranged in a matrix fashion in a display region DSP on an insulating substrate. Disposed around the display region DSP are a drain-side pixel-driving circuit including a drain shift register DSR, a digital-to-analog converter circuit DAC, a drain level shifter DLS, a buffer BF and sampling switches SSW; and a gate-side pixel-driving circuit including a gate shift register GSR and a gate level shifter GLS, and various kinds of circuits. Current mobility of thin film transistors constituting a circuit region SX requiring high-speed operation of these pixel-driving circuits is improved by optimizing a combination of plural layouts, arrangements and configurations for the respective circuits to meet the specifications special for the respective circuits.